REMARKS

Claims 1, 2 and 11 have been amended. Claims 1-18 are currently pending in the application. In view of the foregoing amendments and the remarks that follow, Applicants respectfully request reconsideration.

Independent Claim 10

Independent Claim 10 stands rejected under 35 U.S.C. §102 as anticipated by newly-cited Ma U.S. Patent No. 6,025,242. This ground of rejection is respectfully traversed, for the following reasons. The PTO specifies in MPEP §2131 that, in order for a reference to anticipate a claim under §102, the reference must teach each and every element recited in the claim. Claim 10 of the present application recites:

> A method of forming a semiconductor device on a semiconductor substrate featuring a high dielectric constant (high k) gate insulator layer, comprising the steps of:
>
> forming said high k gate insulator layer on said semiconductor substrate;
>
> forming a conductive gate structure overlying a first area of said high k gate insulator layer;
>
> depositing an insulator layer;
>
> performing a dry etch procedure to first define first insulator spacers on the sides of said conductive gate structure via etching of said insulator layer, and then to remove exposed portions of said high k gate dielectric layer, wherein said exposed portions of said high k gate insulator layer are portions not covered

by said conductive gate structure or by said first insulator spacers; . . . .

As explained in the "Description of Prior Art" section on pages 1-2 of the present application, the semiconductor device fabrication industry has moved toward the use of transistor gate dielectrics that have a relatively high dielectric constant "k", and that are commonly referred to as "high k" dielectric materials. As also explained on pages 1-2, standard dielectric materials (such as silicon dioxide) are much easier to remove from a device than high k dielectric materials. In fact, the traditional process for removing a standard dielectric such as silicon dioxide is not fully effective to remove a high k dielectric. Consequently, an expensive additional process step has traditionally been needed in order to remove unwanted portions of a high k gate dielectric layer prior to source/drain formation. As discussed on page 2 of the present application, Applicants have developed a device fabrication procedure where a high k material is used as a gate dielectric layer, but where unwanted portions of that high k layer are removed without using the additional and expensive process step. A further consideration is that, if the high k gate dielectric layer is removed after the first insulator spacers are formed, the short channel effect of the resulting transistor is improved.

The current §102 rejection of Claim 10 is based on the embodiment shown in Figures 1-6 of the newly-cited Ma patent, where the gate dielectric layer 2 is not a high k material, but instead is made of silicon dioxide (lines 21-23 in column 2). Ma thus did not face the particular problem to which the present invention is directed. Ma does not mention this particular problem, and does not disclose any solution to it. Moreover, since Claim 10 expressly recites a high k dielectric material, and since Figures 1-6 of the patent do not disclose a high k gate dielectric, Ma clearly fails to disclose each and every element that is recited in Applicants' Claim 10. Accordingly, Ma does not anticipate Claim 10 under §102. Claim 10 is therefore believed to be allowable, and notice to that effect is respectfully requested.

Independent Claim 1

Independent Claim 1 recites:

> forming a high dielectric constant (high k) gate dielectric layer on said semiconductor substrate;
>
> forming a conductive gate structure on a first area of said gate dielectric layer;
>
> forming first insulator spacers on the sides of said conductive gate structure with the procedure used to form said first insulator spacers also removing a second area of said gate dielectric layer, wherein said second area of said gate dielectric layer is not covered by said conductive gate structure or by said first insulator spacers; . . . .

Claim 1 stands rejected under 35 U.S.C. §102(b) as anticipated by the Ma patent. The rationale offered for the rejection of Claim 1 is similar to the rationale offered for the rejection of Claim 10. Accordingly, for reasons similar to those discussed above in association with Claim 10, it is respectfully submitted that Claim 1 is patentably distinct from Ma, and notice to that effect is respectfully requested.

Dependent Claims

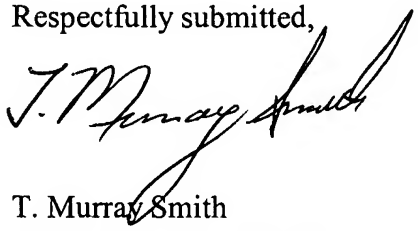
Claims 2-9 and Claims 11-18 respectively depend from Claim 1 and Claim 10, and are also believed to be distinct from the art of record, for example for the same reasons discussed above with respect to Claims 1 and 10.

Conclusion

Based on the foregoing, it is respectfully submitted that all of the pending claims are fully allowable, and favorable reconsideration of this application is therefore respectfully requested. If the Examiner believes that examination of the present application may be advanced in any way by a telephone conference, the Examiner is invited to telephone the undersigned attorney at 972-739-8647.

Although Applicants believe that no fee is due in association with the filing of this Response, the Commissioner is hereby authorized to charge any additional fee required by this paper, or to credit any overpayment, to Deposit Account No. 08-1394 of Haynes and Boone LLP.

Respectfully submitted,



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